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DESCRIPTION

The PT2033 is 2.1 CH Audio Processor by I^2C bus interface. The IC is also a sound processor includes all of the functions required to process the audio signal for TV & Mini Compo, such as Tone control, Volume, Mute, Balance, Loudness, 3 Stereo inputs selector, 1 Stereo output, and 1 Subwoofer out are all built into a single chip to provide Audio system having the highest audio performance and reliability.

FEATURES

- CMOS technology
- Controlled by I²C bus micro-processor interface
- 3 Stereo inputs with selectable input gain
- 2 Channels electronic volume: 0 to -78.75dB, 1.25dB/step
- 1 Subwoofer output: 0 to -37.5dB, 1.25dB/step
- Tone control (Bass and Treble): -14 to +14dB, 2dB/step
- Input gain control: 0 / +11.25dB, 3.75dB/step
- Low distortion
- Low noise and DC stepping
- 32-pin DIP/SOP package

APPLICATIONS

- TV
- Mini compo
- Multimedia speaker

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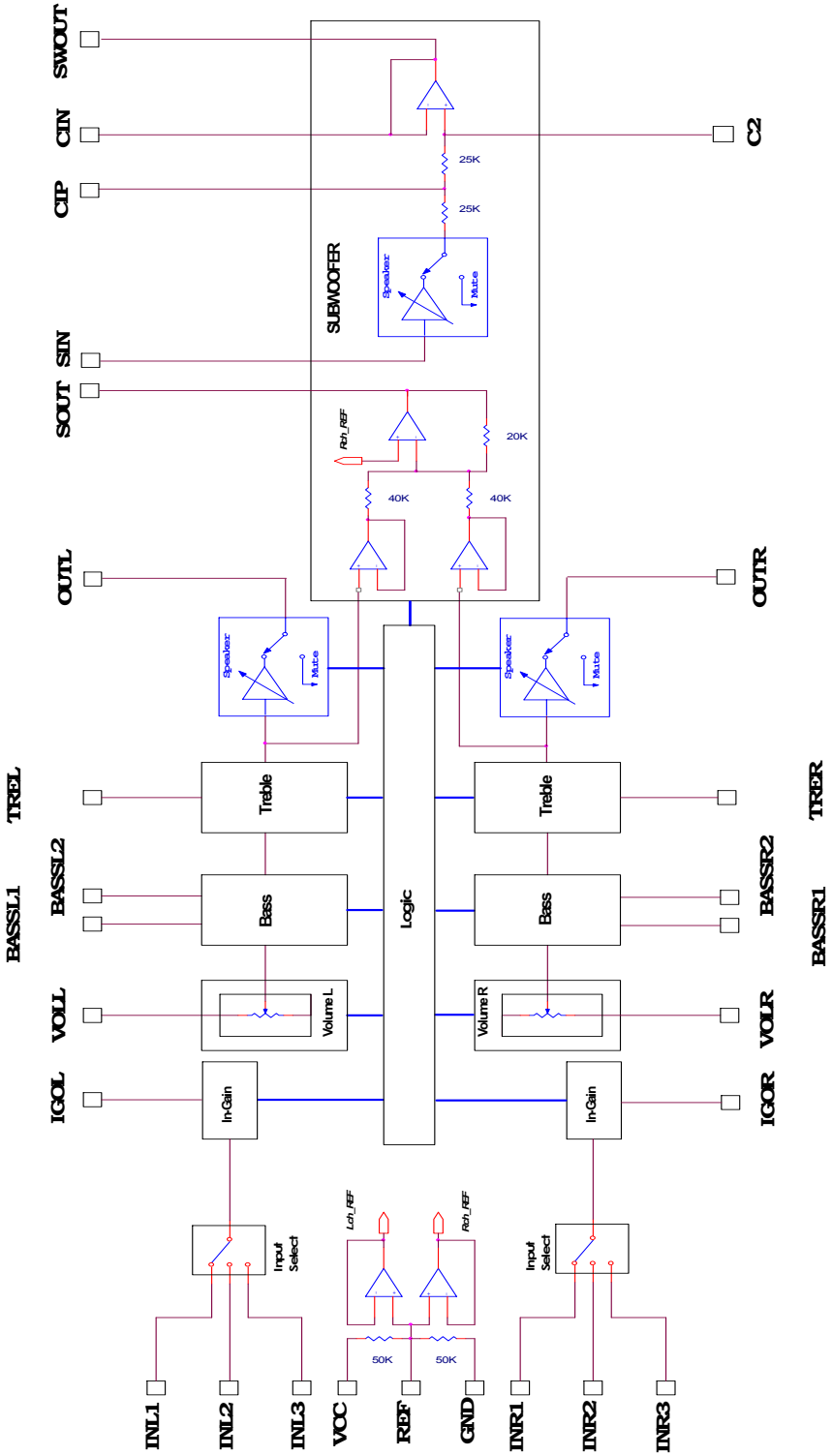
BLOCK DIAGRAM



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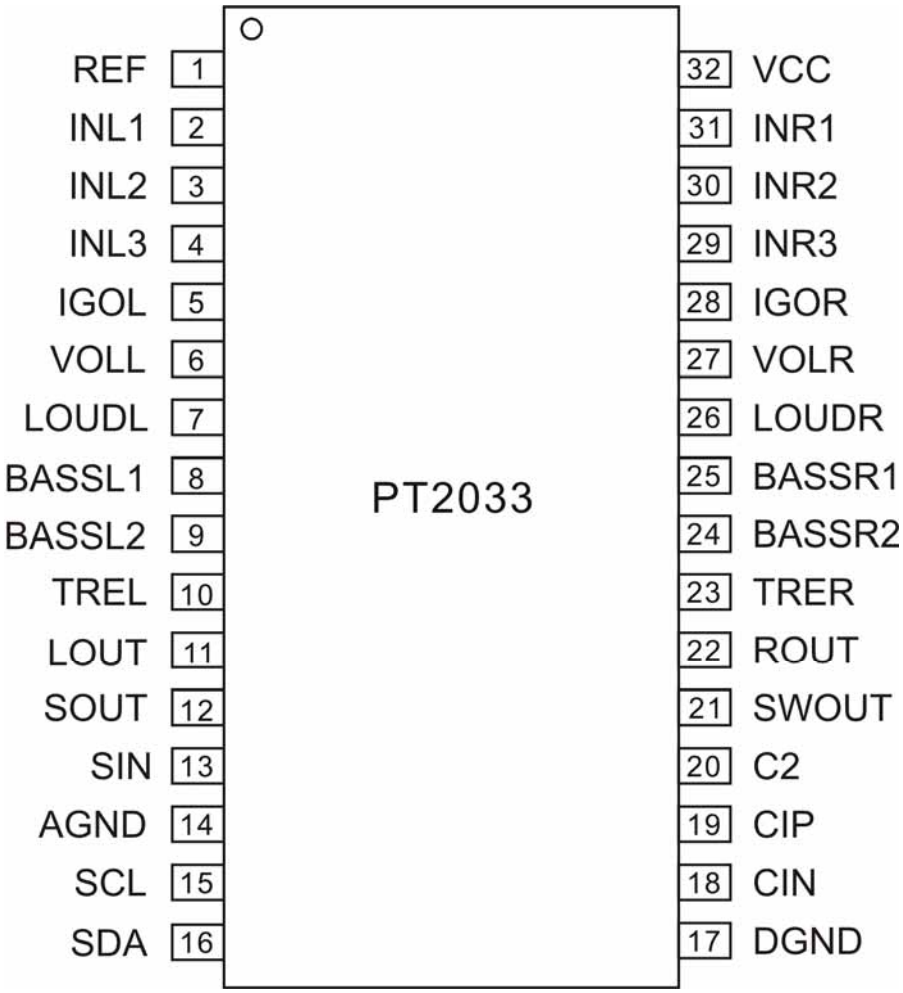
PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
REF	-	Analog reference voltage (1/2 VDD)	1
INL1	I	Left channel input 1	2
INL2	I	Left channel input 2	3
INL3	I	Left channel input 3	4
IGOL	O	Gain output and input selector for left channel	5
VOLL	I	Audio processor left channel input	6
LOUDL	I	Left channel loudness input	7
BASSL1	I	Left channel input for bass controller	8
BASSL2	O	Left bass controller output channel	9
TREL	I	Left channel input for treble controller	10
LOUT	O	Left speaker output	11
SOUT	O	R + L output	12
SIN	I	Low pass filter input	13
AGND	I	Analog ground	14
SCL	I	SCL input	15
SDA	I	SDA input	16
DGND	I	Digital ground	17
CIN	I	Low pass filter external capacitor pin	18
CIP	I	Low pass filter external capacitor pin	19
C2	I	Low pass filter external capacitor pin 2	20
SWOUT	O	Subwoofer channel output pin	21
OUTR	O	Right speaker output	22
TREL	I	Left channel input for treble controller	23
BASSR2	O	Right bass controller output channel	24
BASSR1	I	Right channel input for bass controller	25
LOUDR	I	Right channel loudness input	26
VOLR	I	Audio processor right channel input	27
IGOR	O	Gain output and input selector for right channel	28
INR3	I	Right channel input 3	29
INR2	I	Right channel input 2	30
INR1	I	Right channel input 1	31
VCC	-	Supply input voltage	32

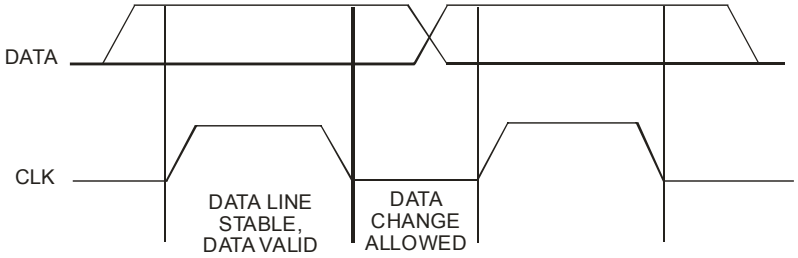
FUNCTIONAL DESCRIPTION

BUS INTERFACE

Data are transmitted to and from the microprocessor to the PT2033 via the DATA and CLK. The DATA and CLK make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

DATA VALIDITY

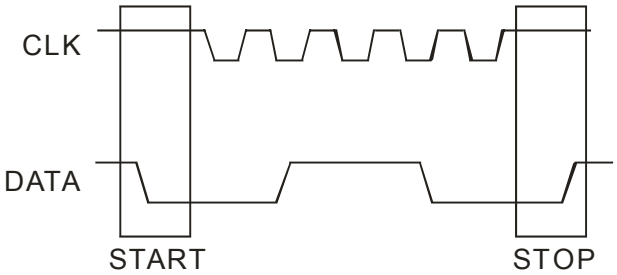
A data on the DATA Line is considered valid and stable only when the CLK Signal is in HIGH State. The HIGH and LOW State of the DATA Line can only change when the CLK signal is LOW. Please refer to the figure below.



START AND STOP CONDITIONS

A Start Condition is activated when
1) the CLK is set to HIGH and
2) DATA shifts from HIGH to LOW State.

The Stop Condition is activated when
1) CLK is set to HIGH and
2) DATA shifts from LOW to HIGH State. Please refer to the timing diagram below.

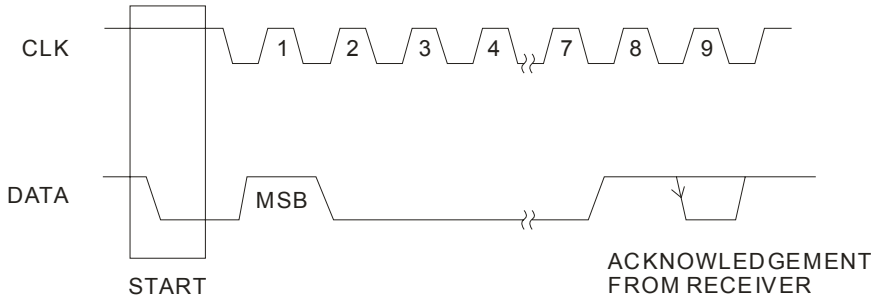


BYTE FORMAT

Every byte transmitted to the DATA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μP) puts a resistive HIGH level on the DATA Line. The peripheral (audio processor) that acknowledges has to pull-down (Low) the DATA line during the Acknowledge Clock Pulse so that the DATA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the DATA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

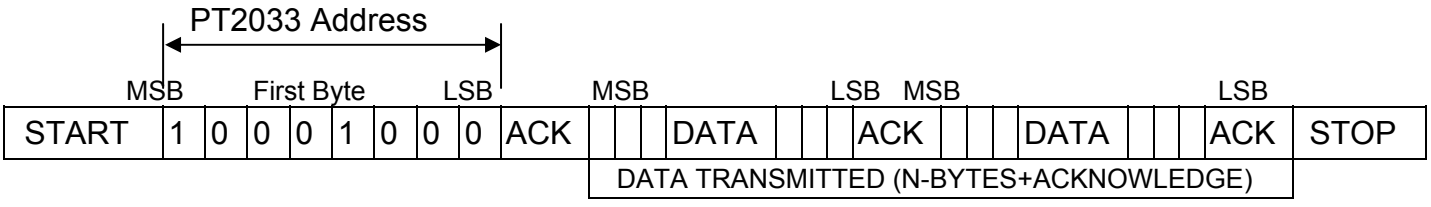
TRANSMISSION WITHOUT ACKNOWLEDGE

If you want to avoid the acknowledge detection of the audio processor, a simpler μP transmission may be used. Wait one clock and does not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

INTERFACE PROTOCOL

The interface protocol consists of the following (see diagram below):

- A Start Condition
- A Chip Address Byte including the PT2033 address. The 8th Bit of the Byte must be “0”. PT2033 must always acknowledge the end of each transmitted byte.
- A Data Sequence (N-Bytes + Acknowledge)
- A Stop Condition



Notes:
ACK=Acknowledge
Max. Clock Speed =100KBITS/S

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SOFTWARE SPECIFICATION

PT2033 ADDRESS

PT2033 Address is shown below.

MSB							LSB
1	0	0	0	1	0	0	0

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT L
1	1	1	B1	B0	A2	A1	A0	Speaker ATT R
1	0	0	B1	B0	A2	A1	A0	Speaker ATT subwoofer
0	1	0	G1	G0	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

where Ax = 1.25 dB/steps; Bx = 10 dB/steps; Cx = 2 dB/steps; Gx = 3.75dB/steps

VOLUME

The table below gives a detailed description of the Volume Data Bytes. For example, a volume of -37.5dB is given by 0 0 0 1 1 1 1 0.

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25 dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

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SPEAKER ATTENUATORS

The table below gives a detailed description of the speaker attenuators data bytes. For example, an attenuation of 30dB on the Speaker R (Right) is given by: 1 1 1 1 1 0 0 0.

MSB							LSB	Function
1	1	0	B1	B0	A2	A1	A0	Speaker L
1	1	1	B1	B0	A2	A1	A0	Speaker R
1	0	0	B1	B0	A2	A1	A0	Speaker ATT subwoofer
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

AUDIO SWITCH DATA BYTE

The following table shows the detailed description of the Audio Switch Data Bytes. For example, a Stereo 1 Input with Gain of +11.25dB Loudness ON is given by: 0 1 0 0 0 0 0 0.

MSB							LSB	Function
0	1	0	G1	G0	S2	S1	S0	Audio switch
						0	0	Stereo 1
						0	1	Stereo 2
						1	0	Stereo 3
						1	1	Stereo 4
					0			Loudness ON
					1			Loudness OFF
			0	0				+11.25dB
			0	1				+7.5dB
			1	0				+3.75dB
			1	1				0dB

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BASS AND TREBLE DATA BYTES

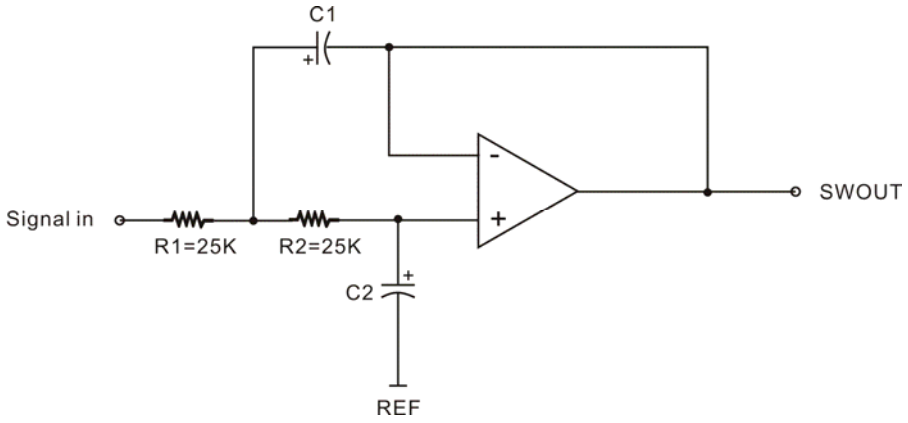
The following table shows a detailed description of the Bass and Treble Data Byte. For example a Treble at -12dB is given by: 0 1 1 1 0 0 0 1.

MSB							LSB	Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

Unit: dB

FILTER

Subwoofer channel mixed from the Main Channel also uses the Sallen Key Type Low Pass Filter to filter out the high frequency characteristics. Two external capacitors can be used to adjust the crossover frequency. Please refer to the diagram below.



The subwoofer in this 3-speaker system has only one channel output; therefore, it is recommended that the LPF must be less than 300Hz. If the frequency is greater than 300Hz, then the audio output is can be clearly discernible. That is, it is easy to know where the sound is coming from. The following diagram provides the suggested crossover frequencies and respective external capacitors.

$$\frac{V_o}{V_i} = \frac{1}{S^2 C_1 C_2 R_1 R_2 + S C_2 (R_1 + R_2) + 1}$$

$$= \frac{\dfrac{1}{C_1 C_2 R_1 R_2}}{S^2 + S\dfrac{1}{C_1 (R_1 // R_2)} + \dfrac{1}{C_1 C_2 R_1 R_2}}$$

Notes:
Crossover Frequency: 218Hz, C1=0.047µF, C2=0.018µF
Crossover Frequency: 148Hz, C1=0.068µF, C2=0.027µF
Crossover Frequency: 92Hz, C1=0.1µF, C2=0.047µF
C1 and C2 are the Low Pass Filter External Capacitors

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Operating supply voltage	Vs	10.5	V
Operating temperature	Topr	-40 to +85	℃
Storage temperature	Tstg	-65 to +150	℃

QUICK REFERENCE DATA

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vs	6	9	10	V
Max. input signal handling	VCL	2	2.5	-	Vrms
Total harmonic distortion (V=1Vrms, f=1KHz)	THD	-	0.03	0.07	%
Signal to noise ratio	S/N	-	95	-	dB
Channel separation (f=1KHz)	Sc	-	85	-	dB
Volume control 1.25dB step	-	-75	-	0	dB
Bass & treble control 2dB step	-	-14	-	+14	dB
Balance control 1.25dB step	-	-37.5	-	0	dB
Subwoofer control 1.25dB step	-	-37.5	-	0	dB
Input gain 3.75dB step	-	0	-	11.25	dB
Mute attenuation	-	-	95	-	dB

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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified: Ta=25℃, Vc=9V, RL=100KΩ, Rg=600Ω, all controls flat (G=0), f=1KHz)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply						
Supply voltage	Vcc	-	6	9	10	V
Supply current	Is	-	-	30	40	mA
Input Selectors						
Input resistance	R_{II}	Input 1,2,3	35	50	65	KΩ
Clipping level	V_{CL}	Av=-8.75 dB ; d=0.3%	2	2.5	-	Vrms
Input separation (2)	S_{IN}	-	80	100	-	dB
Min. input gain	G_{INmin}	-	-1	0	1	dB
Max. input gain	G_{INmax}	-	-	11.25	-	dB
Volume Control						
Control range	C_{RANGE}	-	70	75	80	dB
Min. attenuation	A_{VMIN}	-	-1	0	1	dB
Max. attenuation	A_{VMAX}	-	70	75	80	dB
Step resolution	A_{STEP}	-	0.5	1.25	1.75	dB
Attenuation set error	E_A	AV=0 to -20d	-1.25	0	1.25	dB
		AV=-20 to –60dB	-3.0	-	2	dB
Speaker Attenuators						
Control range	C_{RANGE}	-	35	37.5	40	dB
Step resolution	S_{STEP}	-	0.5	1.25	1.75	dB
Attenuation set error	E_A	-	-	-	1.5	dB
Output mute attenuation	A_{MUTE}	-	90	100	-	dB
Bass Control (1)						
Control range	Gb	Max. Boost/Cut	±12	±14	±16	dB
Step resolution	B_{STEP}	-	1	2	3	dB
Internal feedback resistance	R_B	-	37	47	57	KΩ
Treble Control (1)						
Control range	Gt	Max. Boost/Cut	±13	±14	±15	dB
Step resolution	T_{STEP}	-	1	2	3	dB

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Audio Outputs						
Clipping level	V_{OCL}	d=0.3%	2	2.5	-	Vrms
DC voltage level	V_{OUT}	-	4.2	4.5	4.8	V
General						
Output noise	e_{NO}	BW=20-20KHz, flat output mute all Gain=0dB	-	-100 -95	-	dB
		Output Muted All gains=0dB	-	-98	-	dB
Signal to noise ratio	S/N	All Gains=0dB Vo=1Vrms	-	95	-	dB
Distortion	d	AV=0, Vin=1Vrms	-	0.03	0.07	%
		AV=0, Vin=200Vrms		0.01	0.03	
Channel separation left/right	Sc	-	80	90	-	dB
Crosstalk between bus inputs and signal output	Ct	All Gain=0dB, Vin=1Vrms	85	90	-	dB
Ripple rejection	Rr	Vi(rms)<200mV F=100Hz	-	60	-	dB
Bus Inputs						
Input low voltage	V_{IL}	-	-	-	1	V
Input high voltage	V_{IH}	-	3	-	-	V
Input current	I_{IN}	-	-5	-	+5	μA

Notes:
1. For the Bass and Treble Response, please, refer to the diagram below. The center frequency and quality of the resonance behavior can be selected by the external circuitry. A standard first order bass response can realized by a standard feedback network.
2. The selected input is grounded thru the 2.2μF capacitor.

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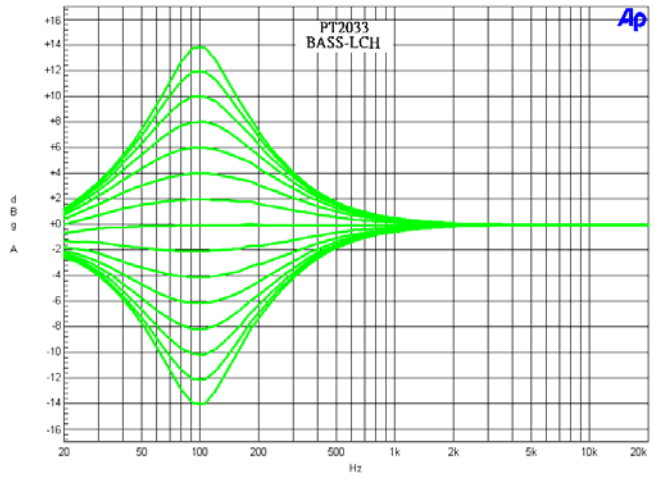
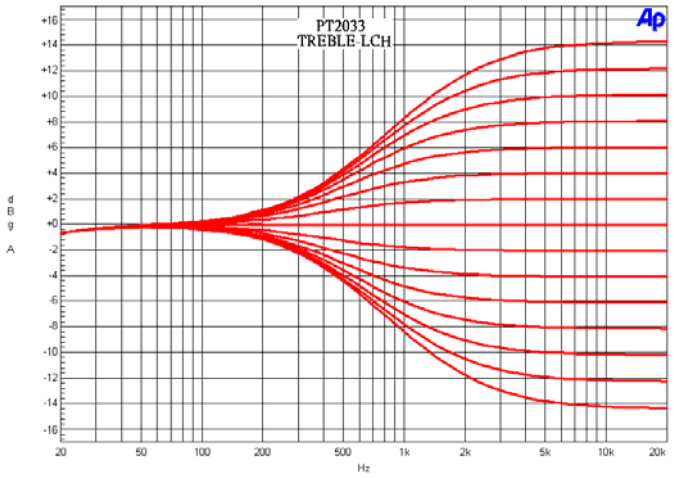
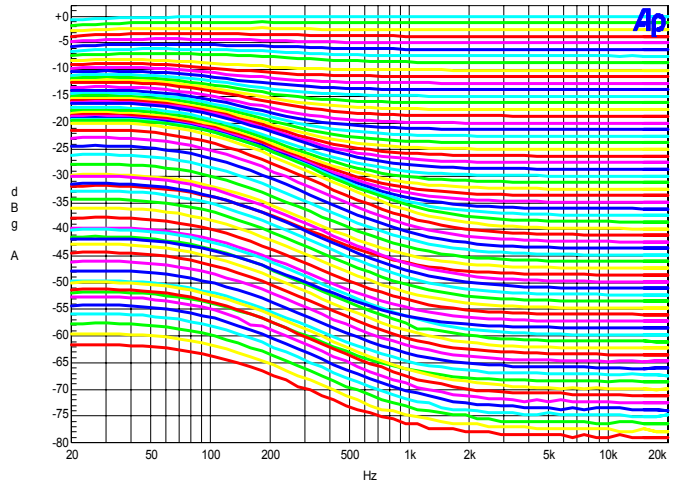


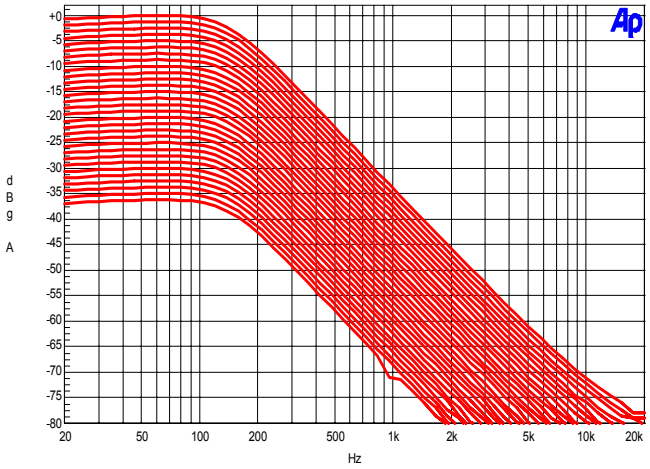
Bass control characteristics



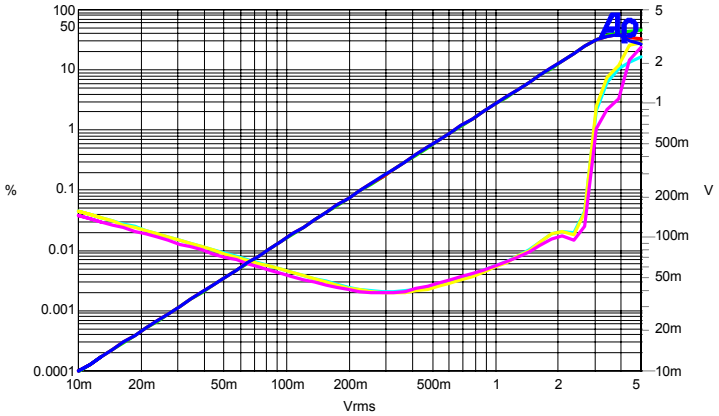
Treble control characteristics



Loudness control characteristics



Subwoofer control characteristics



THD、Output voltage vs. Input voltage

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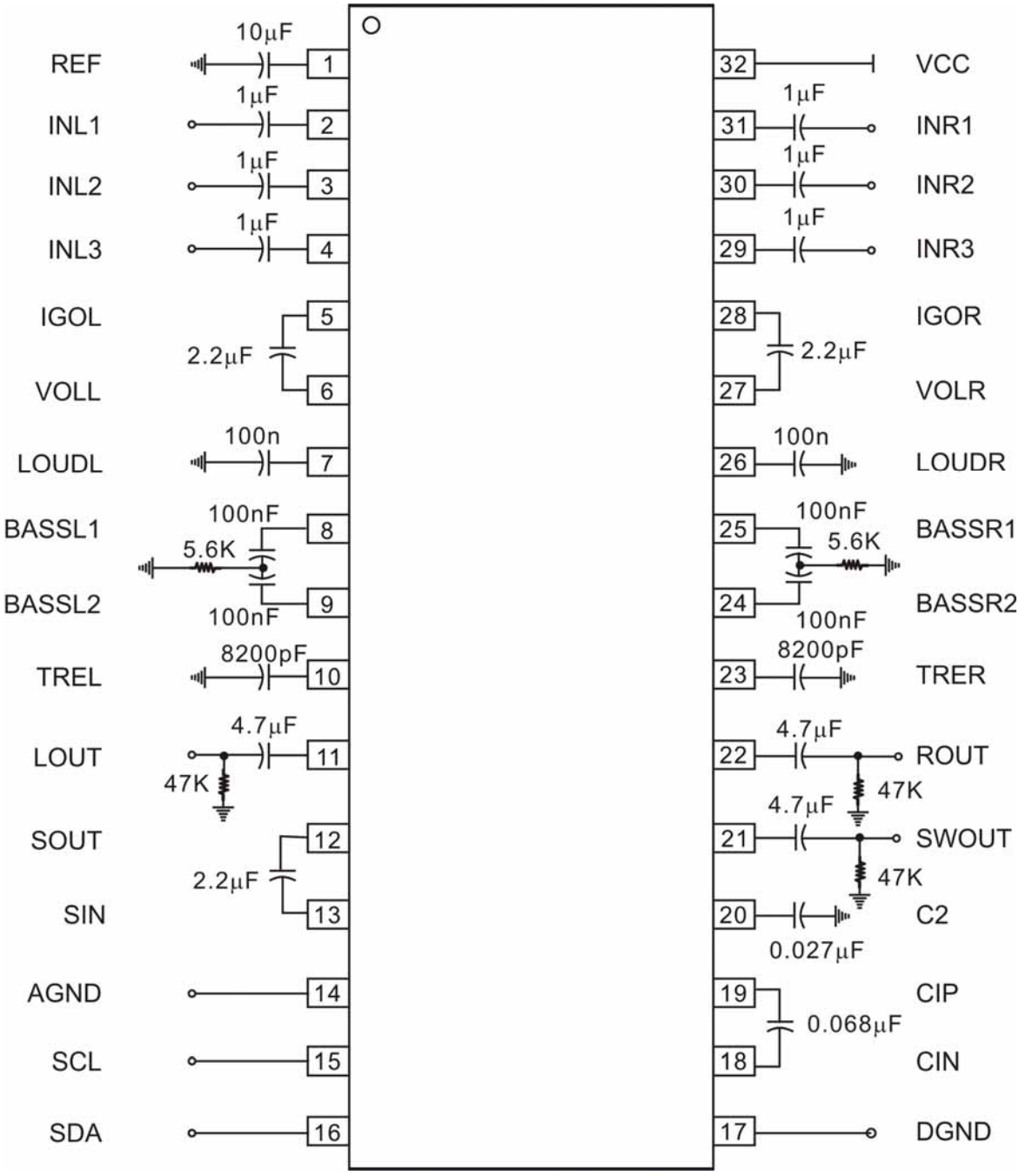
APPLICATION CIRCUIT



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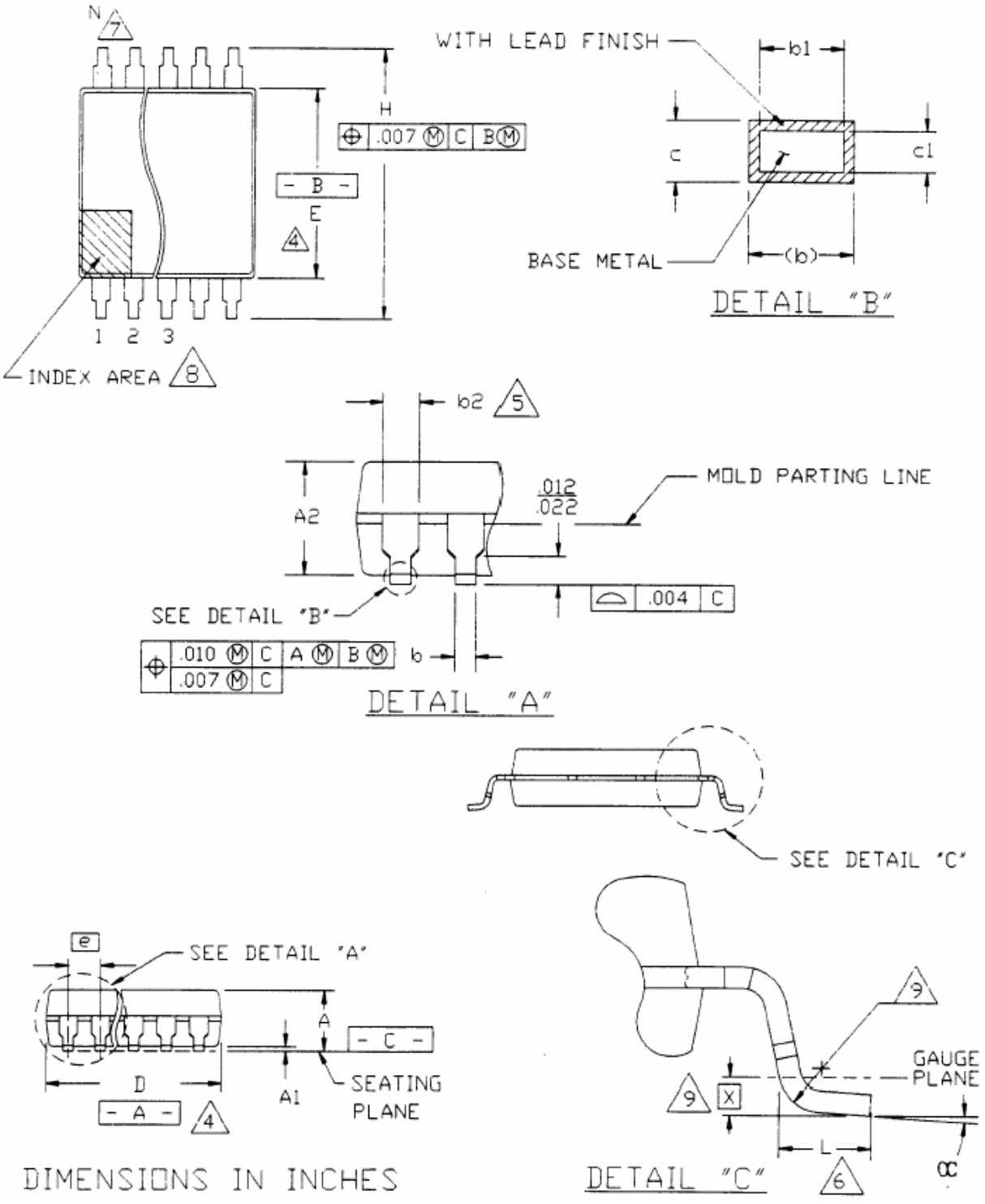
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2033 (L)	32 Pins, SOP, 300mil	PT2033

Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

PACKAGE INFORMATION

32 PINS, SOP, 300MIL



Symbols	Min.	Nom.	Max.
A	-	-	0.104
A1	0.004	-	-
A2	0.082	0.088	0.094
b	0.014	0.016	0.020
b1	0.014	0.016	0.018
b2	0.026	0.028	0.032
c	0.007	0.008	0.0125
c1	0.007	0.008	0.010
D	0.812	0.818	0.824
E	0.292	0.296	0.299
e	0.050 BSC.		
H	0.405	0.412	0.419
L	0.021	0.031	0.041
α	0°	4°	8°

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension E does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. L is the length of the terminal for soldering to a substrate.
6. The lead width B as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in)
7. Controlling dimension: MILLIMETER.
8. N=Number of terminal position (N=32)
9. Refer to JEDEC MO-119 variation AC.

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